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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/211,677	12/14/1998	HYUN CHANG LEE	8733D-7153	9588

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EXAMINER	
NGUYEN, KEVIN M	

ART UNIT	PAPER NUMBER
2674	33

DATE MAILED: 01/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/211,677	LEE, HYUN CHANG	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 10/31/2003 is entered. The rejections of claims 27-84 are maintained.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 82-84 are rejected under 35 U.S.C. 102(e) as being anticipated by Yasui (US 5,784,039).

As to claim 82, Yasui et al teach an active matrix liquid crystal display apparatus comprising: a pixel 4, a switching transistor Qij, a data signal line S1, a gate signal line G1, a data driver 2, a gate driver 3 (see figures 1A and 1B);

the gate driver 3 including means for changing a falling edge (P_G) of the scanning signal (VGi) (see figure 8A);

a data driver connected to the data signal line (S) for applying a data signal (Vs) to the data signal line (S) (see figure 1A and 3A).

As to claim 83, Yasui et al teach the gate signal line drops exponentially over the period of time (t_7 to t_8) (see figure 9); the gate signal line drops linearly over the period of time (see figure 4A); the gate signal line drops stepwise (dV_P, dV_Q) over the period of time from t_1 to t_6 (see figure 10).

As to claim 84, Yasui et al teach the time Δ_1 is so long (fig. 9, col. 14, line 60) and t_{off} is very small Δ_2=0 (fig. 9, col. 15, line 18 and line 22).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 27-33, 36-46, 49-63 and 65-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al (US 5,784,039) in view of Kubota et al (US 5,754,155).

As to claims 27 and 51, Yasui et al teach an active matrix liquid crystal display apparatus associated with a method, the apparatus comprising: a pixel 4, a switching transistor Qij, a data signal line S1, a gate signal line G1, a data driver 2, a gate driver 3, a first voltage source V_{GH}, a second voltage source V_{GL} (see figures 1A and 1B), a switch Swi (figure 7), a gate controller 3 (see figure 6C);

the gate signal line (G1) is electrically connected to the gate electrode (G) of the transistor (TFT) (see fig. 1A and 1B);

a data driver (a source driver 2, see fig. 1A), the data signal line (S1) is electrically connected to the source electrode (S) of the transistor (TFT) (see fig. 1A and 1B);

the gate controller 3 applies gate control signal that cause the gate driver 3 to apply the first voltage V_{GH} to the gate signal line Gi *during the data signal (Vs) to the pixel electrode (C_{LC}) through the data signal line (S)* (see figures 1A and 3A);

the gate controller 3 applies gate control signal that cause the gate driver 3 to apply the second voltage V_{GL} to the gate signal line Gi after the application of the first signal voltage V_{GH}, *but during the application of the data signal (Vs) to the pixel electrode (C_{LC}) through the data signal line (S)* (see figures 1A and 3B);

Yasui et al fail to teach applying a reference potential to the gate signal line after the application of the second signal voltage. However, Kubota et al teach a related active matrix liquid crystal display apparatus which includes applying the reference voltage ($V_{GH'}$, $V_{GL'}$) (12a) to the gate signal line after the application of the second signal voltage (V_{GH} V_{GL}) (see figure 2, column 9, lines 53-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the reference voltage circuit ($V_{GH'}$, $V_{GL'}$)(12a) after the application of the second signal voltage (V_{GH},V_{GL}) taught by Kubota et al for the gate voltage source (V_{GH}, V_{GL}) disclosed in the TFT-LCD device of Yasui et al because this would display an image with high quality

and excellent ability while fabricating a gate driver lower prices (column 6, lines 5-8 of Kubota et al).

6. **As to claim 38**, Yasui et al teach a liquid crystal display device comprising: a plurality of pixels 4, a switching transistor Qij, a plurality of data signal lines S1...Sn, a plurality of scanning signal lines G1...Gm+1, a data driver 2, a gate driver 3, a first voltage source V_{GH}, a second voltage source V_{GL} (see figures 1A and 1B), a plurality of switches Swi to Swi+n (figure 7), a gate driver 3 (see figure 6C);

the gate driver (3) outputs the first voltage V_{GH} on a selected gate line during the application of a data signal in response to a scanning clock signal $-t_0<t<t_1$ (see figure 3A);

the gate driver (3) outputs the second voltage V_{GL} on a selected gate line during the application of a data signal in response to a scanning clock signal $t_1<t<t_2$ (see figure 3B);

Yasui et al fail to teach the gate driver outputs a applying a reference potential after the application of the second signal voltage. However, Kubota et al teach a related LCD device which includes applying the reference voltage ($V_{GH'}$, $V_{GL'}$) (12a) to the gate signal line after the application of the second signal voltage (V_{GH} V_{GL}) (see figure 2, column 9, lines 53-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the reference voltage circuit ($V_{GH'}$, $V_{GL'}$)(12a) after the application of the second signal voltage (V_{GH}, V_{GL}) taught by Kubota et al for the gate voltage source (V_{GH}, V_{GL}) disclosed in the LCD device of Yasui et al because this

would display an image with high quality and excellent ability while fabricating a gate driver lower prices (column 6, lines 5-8 of Kubota et al).

7. **As to claims 56, 62, 71 and 76,** Yasui et al teach an active matrix liquid crystal display device associated with a method, the apparatus comprising: a plurality of pixels 4, a switching transistor Qij, a plurality of data signal lines S1...Sn, a plurality of gate signal lines G1...Gm+1, a data driver 2, a gate driver 3, a first voltage source V_{GH}, a second voltage source V_{GL} (see figures 1A and 1B), a plurality of switches Swi to Swi+n (figure 7), a gate driver 3 (see figure 6C);

the gate driver (3) receiving the first voltage V_{GH} on a selected gate line during the application of a data signal in response to a scanning clock signal $-t_0<t<t_1$ (see figure 3A);

the gate driver (3) receiving the second voltage V_{GL} on a selected gate line during the application of a data signal in response to a scanning clock signal $t_1<t<t_2$ (see figure 3B);

Yasui et al fail to teach "said first gate voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching transistor prior to transition to the second gate voltage, wherein the second gate voltage has a voltage level that turns off the switching transistor." However, Kubota et al teach a related active matrix liquid crystal display apparatus which includes

$$V_{GH'} > V_{sat} + V_{on(PIX)} \text{ by only } V_{th(PIX)}$$

$$V_{GL'} > -V_{sat} - V_{off(PIX)} \text{ by only } V_{th(PIX)}$$

relying to the claimed limitation the first gate voltage V_{sat} + $V_{on(PIX)}$ reducing a voltage level substantially to a threshold voltage level $V_{th(PIX)}$ but enough to maintain an on-state $V_{on(PIX)}$ of the switching transistor $TR_{(PIX)}$ prior to transition to the second gate voltage $-V_{sat} - V_{off(PIX)}$, wherein the second gate voltage $-V_{sat} - V_{off(PIX)}$ has a voltage level that turns off $V_{off(PIX)}$ the switching transistor $TR_{(PIX)}$ (see figure 2, column 9, lines 20-30).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize $V_{GH'} > V_{sat} + V_{on(PIX)}$ by only $V_{th(PIX)}$ and $V_{GL'} > -V_{sat} - V_{off(PIX)}$ by only $V_{th(PIX)}$ taught by Kubota et al for the gate voltage source (V_{GH}, V_{GL}) disclosed in the TFT-LCD device of Yasui et al because this would display an image with high quality and excellent ability while fabricating a gate driver lower prices (column 6, lines 5-8 of Kubota et al).

As to claims 28, 41, 57, Yasui et al teach the gate signal line has a potential that drops from the first voltage to the second voltage over a period of time (see figure 4A).

As to claims 29, 42, 53, 58, 78, Yasui et al teach the gate signal line drops exponentially over the period of time (t_7 to t_8) (see figure 9).

As to claims 30, 43, 54, 59, 79, Yasui et al teach the gate signal line drops linearly over the period of time (see figure 4A).

As to claims 31, 44, 55, 60, 80, Yasui et al teach the gate signal line drops stepwise (dV_P, dV_Q) over the period of time from t_1 to t_6 (see figure 10).

As to claims 32, 45, 52, 61, 77, Yasui et al teach the first voltage (V_{GH}) is greater than a second voltage (V_{GL}) (see figure 10).

As to claims 33, 46, Yasui et al teach the gate controller 3 including a timing controller (t).

As to claims 36, 49, Yasui et al teach the first voltage is applied before the data signal is applied (see figure 3A).

As to claims 37, 50, Yasui et al teach the second voltage (V_{GL}) is ground (see figure 3A).

As to claim 39, Yasui et al teach the gate driver 3 sequentially changed the selected gate line Gi (see figure 3).

As to claim 40, Yasui et al teach the gate driver 3 includes a switch SWi that selectively provides the first voltage and the second voltage to the selected gate line (see figure 7).

As to claim 63, Yasui et al teach the first gate voltage V_{GH} is supplied to the gate lines Gi during a time interval –t0<t<t1 when the thin film transistors TFT connected to the gate lines are turned on (see figure 3A).

As to claims 65, 68, 69, 70, 81, Kubota et al teach the first gate voltage V_{sat} + $V_{on(PIX)}$ reducing a voltage level substantially to a threshold voltage level $V_{th(PIX)}$ prior to excitation of successive gate signal line (see figure 2).

As to claims 66, 67, 72-75, Yasui et al teach a voltage controller comprising the switch Swi (see figure 7) and a low level gate voltage generator $-V_{sat} - V_{off(PIX)}$, and switch $TR_{(PIX)}$ (see figure 2).

8. Claims 35 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al in view Kubota et al, and further in view of Applicant's Admitted Prior Art hereinafter AAPA.

As to claims 35 and 48, Yasui et al and Kubota et al teach all of the claimed limitation of claims 27 and 38, except for the gate signal line includes a distributed series resistance and a distributed capacitance. However, AAPA discloses the gate signal line includes a distributed series resistance R1 and a distributed capacitance C1 (see figure 3, page 5, lines 2-5). Since a waveform modifying circuit such as an integrator for each gate line must be added (page 5, lines 30-32). Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the gate signal line includes a distributed series resistance R1 and a distributed capacitance C1 disclosed by AAPA in Yasui et al's scanning line of TFT-LCD device because this would eliminate flickering and residual image (see page 5, lines 29-30 of AAPA).

9. Claims 34, 47 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui et al in view Kubota et al, and further in view of Hirai et al (US 5,646,643).

As to claims 34, 47 and 64, Yasui et al and Kubota et al teach all of the claimed limitation of claims 27, 38 and 62, except for the shift register. However, Hirai et al teach a register 707 controlling the switching section 709 (see figure 8). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize a register 707 taught by Hirai et al in Yasui et al's and Kubota et al's gate driver because this would provide high grade of image display by a simple and inexpensive means of

solving a drawback of display fluctuation or crosstalk on a display in the LCD device (column 8, lines 32-35 of Hirai et al).

Response to Arguments

10. Applicant's arguments filed 10/31/2003 have been fully considered but they are not persuasive.

In response to applicant's argument that claim 27 recited [lines 17-19 of claim 27]. This argument is not persuasive because Yasui's invention teaches the gate controller 3 applies gate control signal that cause the gate driver 3 to apply the second voltage V_{GL} to the gate signal line Gi after the application of the first signal voltage V_{GH}, *but during the application of the data signal (Vs) to the pixel electrode (C_{LC}) through the data signal line (S)* (see figures 1A and 3B).

In response to applicant's argument that claims 38 and 51 recited "wherein the second voltage is substantially equal to a potential of the data signal." This argument is not persuasive because how and where in the specification support "the second voltage is substantially equal to a potential of the data signal."

In response to applicant's argument that claims 56, 62, 71 and 76 recited "said first gate voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching transistor prior to transitioning to the second gate voltage, wherein the second gate voltage has a voltage level that turns off the switching transistor." This argument is not persuasive because Kubota's invention teaches a voltage of Vsat+Von(pix) is applied to the source electrode of the transistor

TF(pix) in on of the circuit, and a voltage of –Vsat-Voff(pix) is applied to the source electrode of the transistor TR(pix) in other circuit. Here, Vsat is a saturation voltage of liquid crystal , and Von(pix) and Voff(pix) are respectively an on-margin and an off-margin of the transistor TF(pix).

In response to applicant's argument that claim 82 recited "the gate driver including means for changing a falling edge of the scanning signal." This argument is not persuasive because this would Yasui's invention teaches the gate driver 3 including means for changing a falling edge (P_G) of the scanning signal (VGi) (see figure 8A);

For these reasons, the rejections based on Yasui et al, Kubota et al, AAPA and Hirai et al have been maintained.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

XIAO WU
PRIMARY EXAMINER